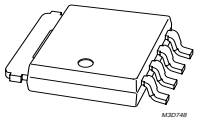


# PH3230

N-channel enhancement mode field-effect transistor

**Rev. 02 — 5 September 2002** **Product data**

## 1. Description

The latest generation N-channel enhancement mode field-effect power transistor in a SOT669 (LFPAK) package.

Product availability:

PH3230 in SOT669 (LFPAK).

## 2. Features

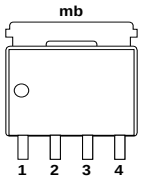
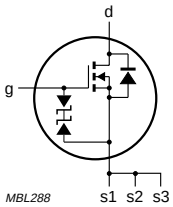
- Logic level compatible
- Low drive current
- High density mounting
- Very low on-state resistance.

## 3. Applications

- DC to DC converter
- Computer motherboards
- Switch mode power supplies.

## 4. Pinning information

**Table 1: Pinning - SOT669 (LFPAK), simplified outline and symbol**

| Pin | Description | Simplified outline | Symbol |
|---|---|---|---|
| 1,2,3 | source (s) |  |  |
| 4 | gate (g) | | |
| mb | mounting base, connected to drain (d) | | |





**SOT669 (LFPAK)**

## 5. Quick reference data

**Table 2: Quick reference data**

| Symbol | Parameter | Conditions | Typ | Max | Unit |
|---|---|---|---|---|---|
| $V_{DS}$ | drain-source voltage (DC) | $T_j$ = 25 °C | - | 30 | V |
| $I_D$ | drain current (DC) | $T_{mb}$ = 25 °C | - | 50 | A |
| $P_{tot}$ | total power dissipation | $T_{mb}$ = 25 °C | - | 42 | W |
| $T_j$ | junction temperature | | - | 150 | °C |
| $R_{DSon}$ | drain-source on-state resistance | $V_{GS}$ = 10 V; $I_D$ = 25 A; $T_j$ = 25 °C | 3.2 | 3.7 | mΩ |
| | | $V_{GS}$ = 4.5 V; $I_D$ = 25 A; $T_j$ = 25 °C | 5.5 | 7.3 | mΩ |

## 6. Limiting values

**Table 3: Limiting values**

*In accordance with the Absolute Maximum Rating System (IEC 60134).*

| Symbol | Parameter | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| $V_{DS}$ | drain-source voltage (DC) | 25 °C ≤ $T_j$ ≤ 150 °C | - | 30 | V |
| $V_{GS}$ | gate-source voltage (DC) | | - | ±20 | V |
| $I_D$ | drain current (DC) | $V_{GS}$ = 10 V; $T_{mb}$ = 25 °C; Figure 2 and 5 | - | 50 | A |
| $I_{DM}$ | peak drain current | $T_{mb}$ = 25 °C; pulsed; $t_p$ ≤ 10 µs; Figure 5 | - | 200 | A |
| $P_{tot}$ | total power dissipation | $T_{mb}$ = 25 °C; Figure 1 | - | 42 | W |
| $T_{stg}$ | storage temperature | | –55 | +150 | °C |
| $T_j$ | junction temperature | | –55 | +150 | °C |
| **Source-drain diode** | | | | | |
| $I_{SM}$ | peak source (diode forward) current | $T_{mb}$ = 25 °C; pulsed; $t_p$ ≤ 10 µs | - | 50 | A |
| **Avalanche ruggedness** | | | | | |
| $I_{DS(AL)R}$ | repetitive drain-source avalanche current | $T_j$ = 25 °C | - | 5 | A |
| $E_{DS(AL)R}$ | repetitive drain-source avalanche energy | $T_j$ = 25 °C; $R_{GS}$ ≥ 50 Ω; $I_{DS(AL)R}$ = 5A; $V_{DD}$ = 15V; duty < 0.1% | - | 2.5 | mJ |



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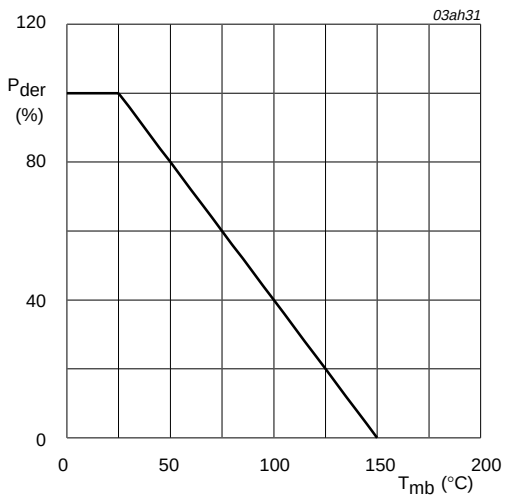
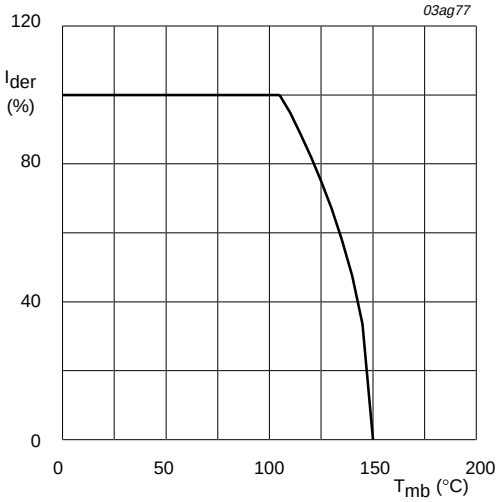



$$P_{der} = \frac{P_{tot}}{P_{tot(25^{\circ}C)}} \times 100\%$$

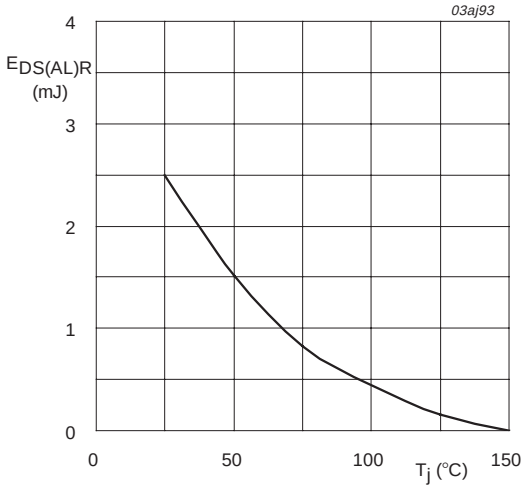
**Fig 1. Normalized total power dissipation as a function of mounting base temperature.**




$V_{GS} \geq 10$ V

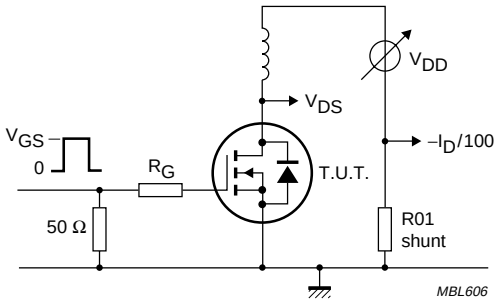
$$I_{der} = \frac{I_D}{I_{D(25^{\circ}C)}} \times 100\%$$

**Fig 2. Normalized continuous drain current as a function of mounting base temperature.**




$I_{AR}$ = 5 A; $V_{DD}$ = 15V; duty< 0.1%; $R_G \geq 50\Omega$

**Fig 3. Repetitive avalanche energy rating.**




$$E_{AR} = 0.5 \times (LI_{AR})^2 \times \frac{V_{DSS}}{V_{DSS} - V_{DD}}$$

**Fig 4. Avalanche energy test circuit.**



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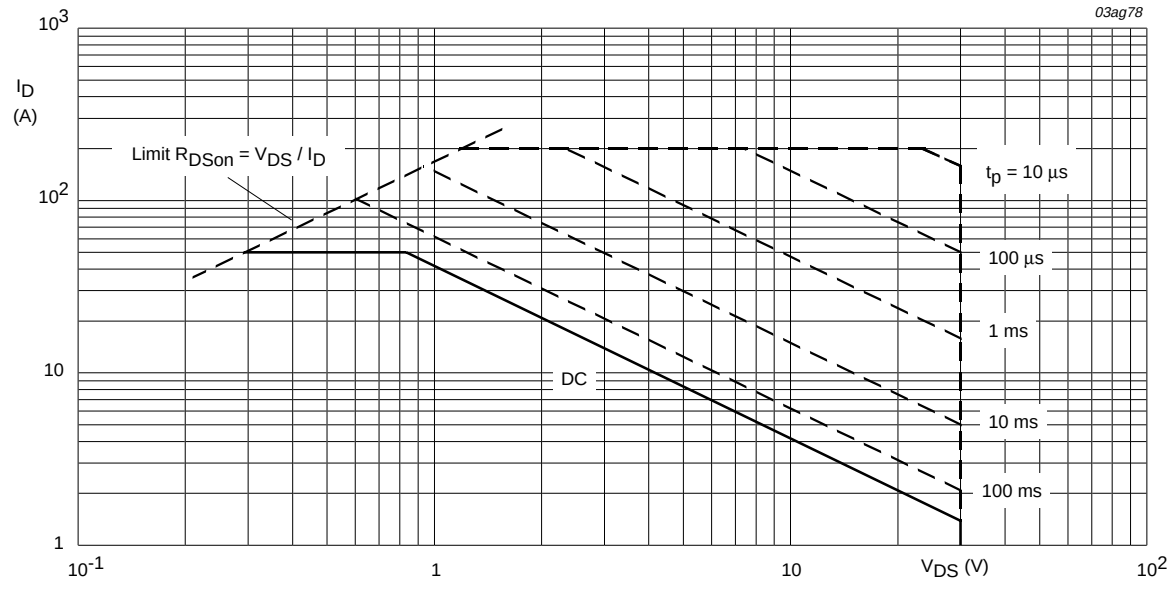


$T_{mb}$ = 25 °C; $I_{DM}$ is single pulse.

**Fig 5. Safe operating area; continuous and peak drain currents as a function of drain-source voltage.**



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# 7. Thermal characteristics

**Table 4: Thermal characteristics**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $R_{th(j-mb)}$ | thermal resistance from junction to mounting base | Figure 6 | - | - | 3 | K/W |

## 7.1 Transient thermal impedance

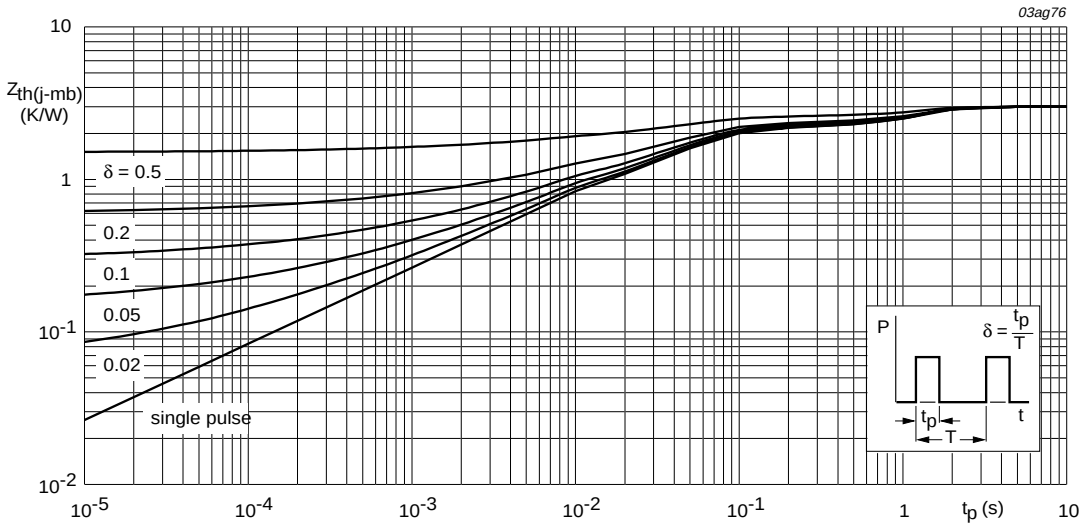


**Fig 6. Transient thermal impedance from junction to mounting base as a function of pulse duration.**



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# 8. Characteristics

**Table 5: Characteristics**

*$T_j$ = 25 °C unless otherwise specified.*

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **Static characteristics** | | | | | | |
| $V_{(BR)DSS}$ | drain-source breakdown voltage | $I_D$ = 10 mA; $V_{GS}$ = 0 V | 30 | - | - | V |
| $V_{GS(th)}$ | gate-source threshold voltage | $I_D$ = 1 mA; $V_{DS}$ = $V_{GS}$; Figure 11 | 1 | 1.9 | 2.5 | V |
| $I_{DSS}$ | drain-source leakage current | $V_{DS}$ = 30 V; $V_{GS}$ = 0 V | - | - | 1 | µA |
| $I_{GSS}$ | gate-source leakage current | $V_{GS}$ = ±16 V; $V_{DS}$ = 0 V | - | 0.1 | 10 | µA |
| $R_{DSon}$ | drain-source on-state resistance | $V_{GS}$ = 10 V; $I_D$ = 25 A; Figure 9 and 10 | - | 3.2 | 3.7 | mΩ |
| | | $V_{GS}$ = 4.5 V; $I_D$ = 25 A; Figure 10 | - | 5.5 | 7.3 | mΩ |
| **Dynamic characteristics** | | | | | | |
| $g_{fs}$ | forward transconductance | $V_{DS}$ = 10 V; $I_D$ = 25 A; Figure 13 | 39 | 55 | - | S |
| $Q_{g(tot)}$ | total gate charge | $I_D$ = 50 A; $V_{DD}$ = 10 V; $V_{GS}$ = 10 V; Figure 16 | - | 75 | - | nC |
| $Q_{gs}$ | gate-source charge | | - | 16 | - | nC |
| $Q_{gd}$ | gate-drain (Miller) charge | | - | 14 | - | nC |
| $C_{iss}$ | input capacitance | $V_{GS}$ = 0 V; $V_{DS}$ = 10 V; f = 1 MHz; Figure 14 | - | 4750 | - | pF |
| $C_{oss}$ | output capacitance | | - | 1160 | - | pF |
| $C_{rss}$ | reverse transfer capacitance | | - | 630 | - | pF |
| $t_{d(on)}$ | turn-on delay time | $V_{DD}$ = 10 V; $I_D$ = 25 A; $V_{GS}$ = 10 V; $R_G$ = 4.7 Ω | - | 25 | - | ns |
| $t_r$ | rise time | | - | 50 | - | ns |
| $t_{d(off)}$ | turn-off delay time | | - | 90 | - | ns |
| $t_f$ | fall time | | - | 26 | - | ns |
| **Source-drain (reverse) diode** | | | | | | |
| $V_{SD}$ | source-drain (diode forward) voltage | $I_S$ = 50 A; $V_{GS}$ = 0 V; Figure 15 | - | 0.85 | 0.98 | V |
| $t_{rr}$ | reverse recovery time | $I_S$ = 50 A; $dI_S/dt$ = –50 A/µs; $V_{GS}$ = 0 V | - | 60 | - | ns |



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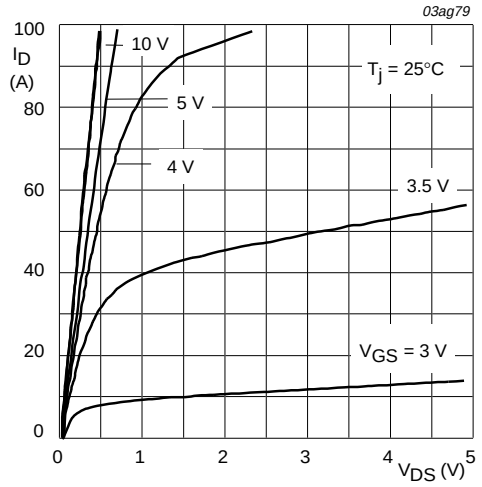
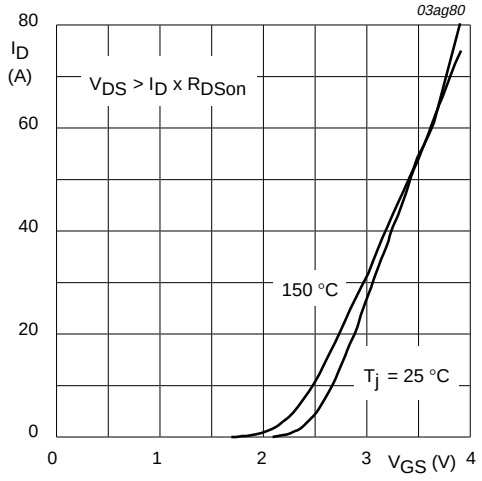


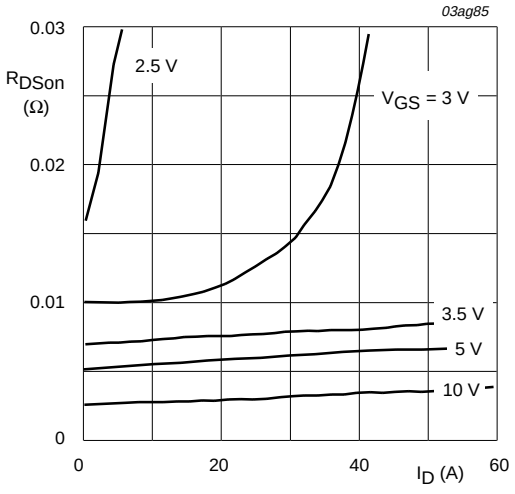

$T_j$ = 25 °C

**Fig 7. Output characteristics: drain current as a function of drain-source voltage; typical values.**



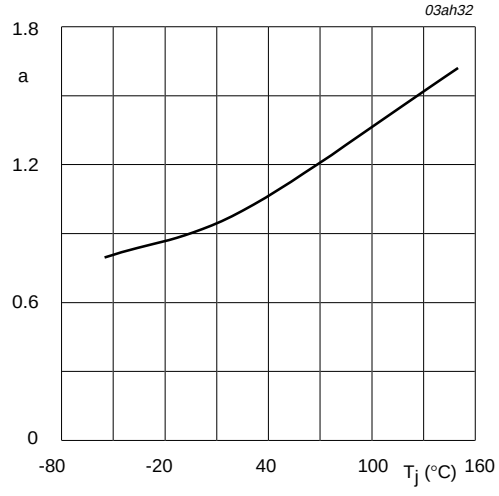

$T_j$ = 25 °C and 150 °C; $V_{DS} > I_D \times R_{DSon}$

**Fig 8. Transfer characteristics: drain current as a function of gate-source voltage; typical values.**




$T_j$ = 25 °C

**Fig 9. Drain-source on-state resistance as a function of drain current; typical values.**




$$a = \frac{R_{DSon}}{R_{DSon(25°C)}}$$

**Fig 10. Normalized drain-source on-state resistance factor as a function of junction temperature.**



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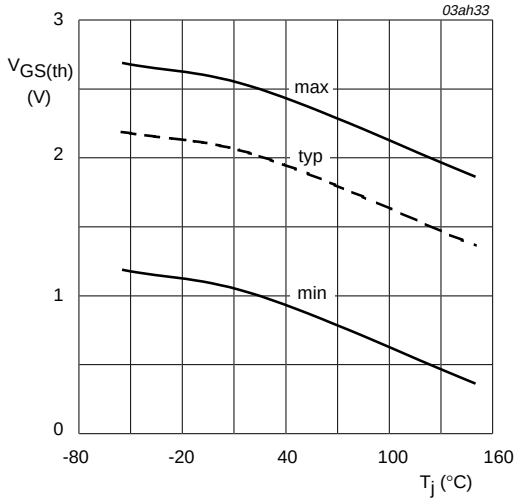
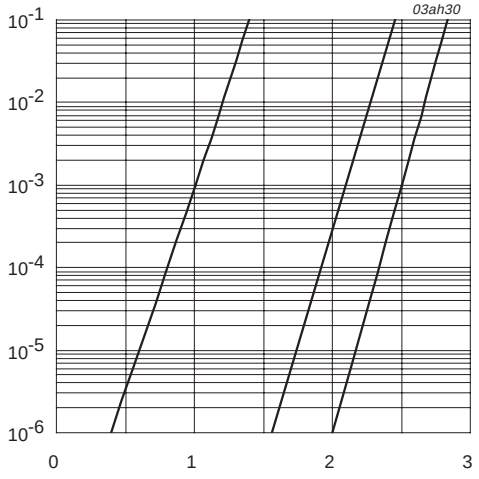


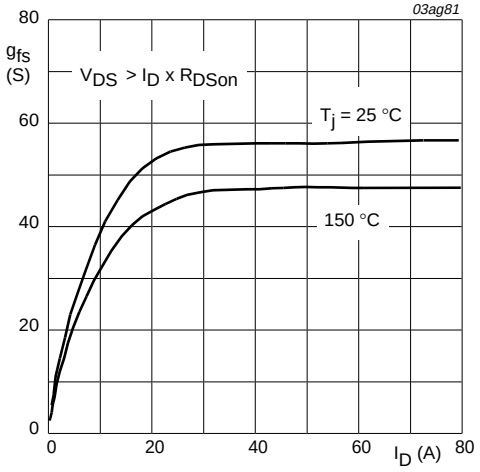

$I_D$ = 1 mA; $V_{DS}$ = $V_{GS}$

**Fig 11. Gate-source threshold voltage as a function of junction temperature**



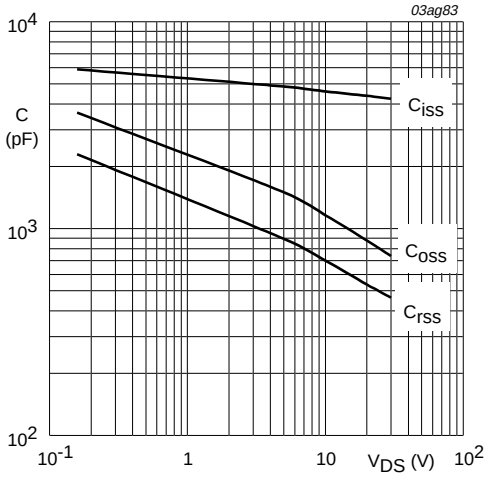

$T_j$ = 25 °C

**Fig 12. Sub-threshold drain current as a function of gate-source voltage.**




$T_j$ = 25 °C and 150 °C; $V_{DS} > I_D \times R_{DSon}$

**Fig 13. Forward transconductance as a function of drain current; typical values.**




$V_{GS}$ = 0 V; f = 1 MHz

**Fig 14. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values.**



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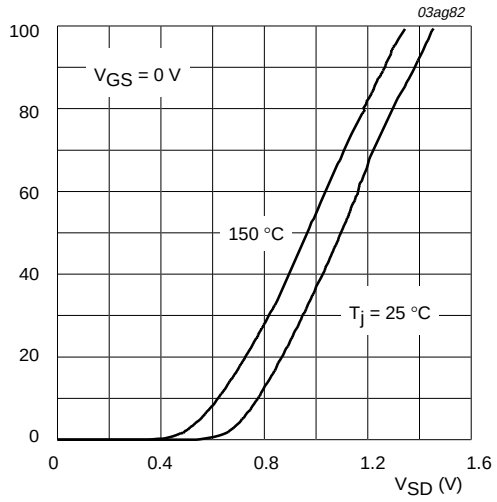
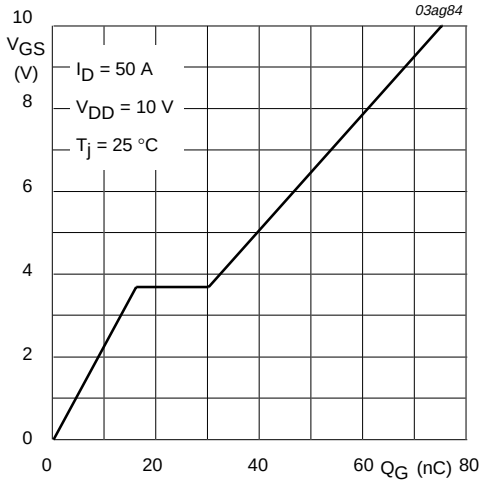



$T_j$ = 25 °C and 150 °C; $V_{GS}$ = 0 V

**Fig 15. Source (diode forward) current as a function of source-drain (diode forward) voltage; typical values.**




$T_j$ = 25 °C; $I_D$ = 50 A; $V_{DD}$ = 10V

**Fig 16. Gate-source voltage as a function of gate charge; typical values.**



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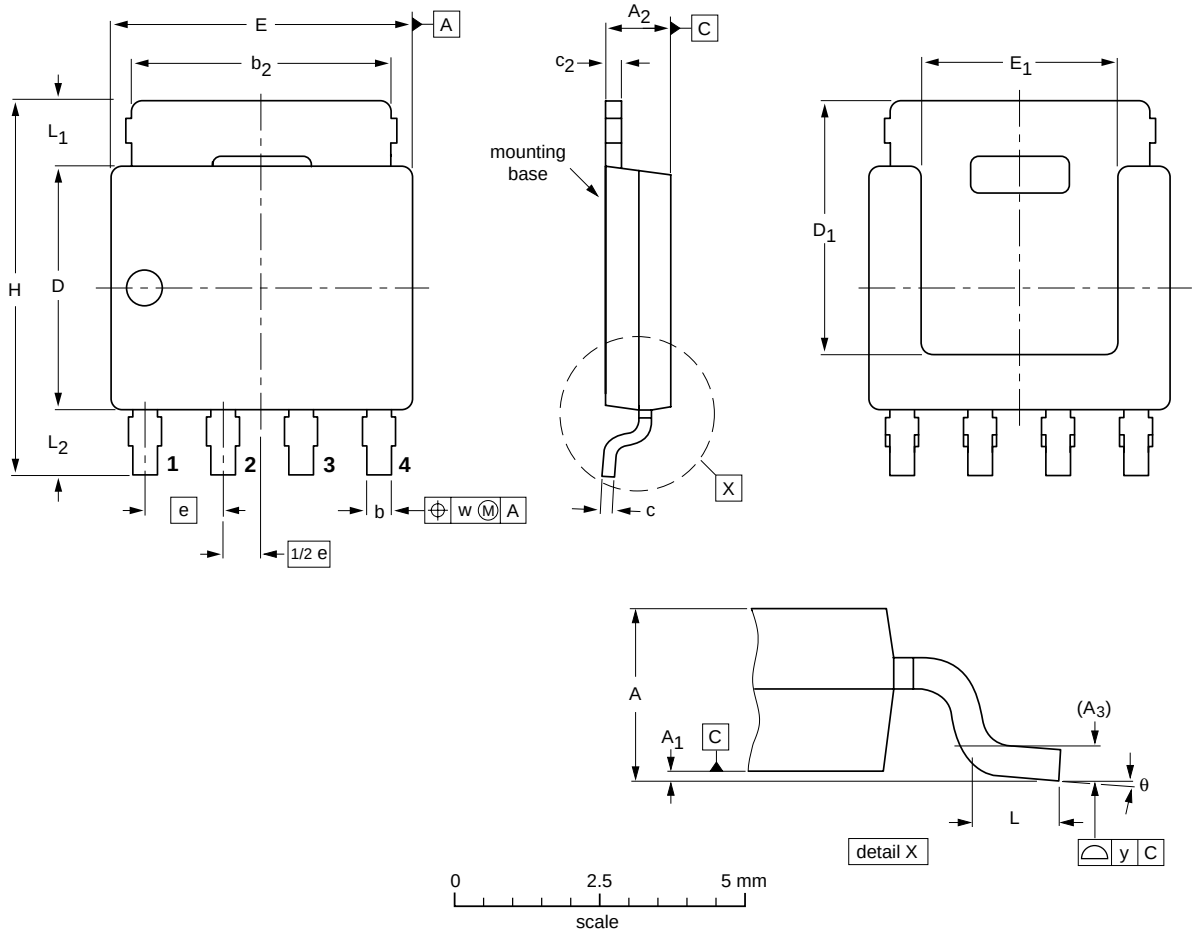
## 9. Package outline

**Plastic single-ended surface mounted package (Philips version LFPAK); 4 leads** **SOT669**




**DIMENSIONS (mm are the original dimensions)**

| UNIT | A | $A_1$ | $A_2$ | $A_3$ | b | $b_2$ | c | $c_2$ | $D^{(1)}$ | $D_1^{(1)}$ max | $E^{(1)}$ | $E_1^{(1)}$ | e | H | L | $L_1$ | $L_2$ | w | y | θ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| mm | 1.20<br>1.01 | 0.15<br>0.00 | 1.10<br>0.95 | 0.25 | 0.50<br>0.35 | 4.41<br>3.62 | 0.25<br>0.19 | 0.30<br>0.24 | 4.10<br>3.80 | 4.20 | 5.0<br>4.8 | 3.3<br>3.1 | 1.27 | 6.2<br>5.8 | 0.85<br>0.40 | 1.3<br>0.8 | 1.3<br>0.8 | 0.25 | 0.1 | 8°<br>0° |

**Note**

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|---|---|---|---|---|---|---|
| | IEC | JEDEC | JEITA | | | |
| SOT669 | | | | | | ~~01-07-18~~<br>02-07-10 |

**Fig 17. SOT669 (LFPAK).**



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## 10. Revision history

Table 6: Revision history

| Rev | Date | CPCN | Description |
|---|---|---|---|
| 02 | 20020905 | | **Product data (9397 750 10122)**<br>Modifications:<br>• Ruggedness graphs and data added. |
| 01 | 20020207 | | **Product data (9397 750 09395)** |


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## 11. Data sheet status

| Data sheet status[1] | Product status[2] | Definition |
|---|---|---|
| Objective data | Development | This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice. |
| Preliminary data | Qualification | This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product. |
| Product data | Production | This data sheet contains data from the product specification. Philips Semiconductors reserves the right to make changes at any time in order to improve the design, manufacturing and supply. Changes will be communicated according to the Customer Product/Process Change Notification (CPCN) procedure SNW-SQ-650A. |

[1] Please consult the most recently issued data sheet before initiating or completing a design.

[2] The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL http://www.semiconductors.philips.com.

## 12. Definitions

**Short-form specification —** The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

**Limiting values definition —** Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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9397 750 10122

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**Date of release: 5 September 2002** **Document order number: 9397 750 10122**

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